LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Withdrawn) A method for fabricating a high-voltage MOS transistor on a substrate, the method comprising:

forming a first doping region with a first dosage in the substrate;

forming a gate structure overlying the substrate and partially covering the first doping region; and

ion implanting the substrate using the gate structure as a mask to simultaneously form a second doping region with a second dosage within the first doping region to serve as a drain region and form a third doping region with the second dosage in the substrate to serve as a source region;

wherein a channel region is formed in the substrate between the first and third doping regions when the high-voltage MOS transistor is turned on to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

2. (Withdrawn) The method as claimed in claim 1, further comprising the step of performing a drive in process on the first doping region.

3. (Withdrawn) The method as claimed in claim 2, wherein the drive in process is performed at 1000 to 1100°C.

4. (Withdrawn) The method as claimed in claim 2, wherein the drive in process i performed for 6 to 8 hours.

5. (Withdrawn) The method as claimed in claim 1, wherein the first dosage is about 7.0 to 9.0E12 ions/cm^2.

6. (Withdrawn) The method as claimed in claim 1, wherein the gate structure is composed of a gate, a gate dielectric layer, and a gate spacer.

7. (Withdrawn) The method as claimed in claim 1, wherein the second dosage is about 2.0 to 4.0E15 ions/cm^2.

8. (Original) A high-voltage MOS transistor comprising:

a substrate;

a gate structure overlying the substrate, the gate structure having a first side and a second side opposite to the first side;

a first doping region with a first dosage formed in the substrate on the first side of the gate structure and partially covered by the gate structure; and

a second doping region with a second dosage formed within the first doping region adjacent to the edge on the first side of the gate structure to serve as a drain region and a third doping region with the second dosage formed in the substrate adjacent to the edge of the second side of the gate structure to serve as a source region;

a channel region formed in the substrate between the first and third doping regions by turning on the high-voltage MOS transistor to pass current between the source and drain regions, where a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

9. (Original) The device as claimed in claim 8, wherein the gate structure is composed of a gate, a gate dielectric layer, and a gate spacer.

10. (Original) The device as claimed in claim 8, wherein the first dosage is about 7.0 to 9.0E12 ions/cm^2.

11. (Original) The device as claimed in claim 10, wherein the second dosage is about 2.0 to 4.0E15 ions/cm^2.

12. (Withdrawn) A method for fabricating a high-voltage MOS transistor, comprising the steps of:

providing a substrate;

forming a masking layer overlying the substrate;

ion implanting the substrate using the masking layer as a mask to form a pair of first doping regions with a first dosage in the substrate;

removing the masking layer;

forming a gate structure overlying the substrate between the pair of first doping regions and partially covering each first doping region; and

ion implanting the substrate using the gate structure as a mask to form a pair of second doping regions with a second dosage within the pair of first doping regions to serve as source and drain regions.

13. (Withdrawn) The method as claimed in claim 12, wherein the masking layer is a photoresist layer.

14. (Withdrawn) The method as claimed in claim 12, further comprising the step of performing a drive in process on the first doping region.

15. (Withdrawn) The method as claimed in claim 14, wherein the drive in process is performed at 1000 to 1100°C.

16. (Withdrawn) The method as claimed in claim 14, wherein the drive in process is performed for 6 to 8 hours.

17-23. (Cancelled)